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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,065	11/19/2003	Douglas D. Coolbaugh	BUR920020116US1	1064
23389	7590	11/17/2004	EXAMINER	
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA GARDEN CITY, NY 11530			GEBREMARIAM, SAMUEL A	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/707,065

Applicant(s)

COOLBAUGH ET AL.

Examiner

Samuel A Gebremariam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding the limitation of at least one wiring region that lies to the periphery of the metal stacked inductor, said wherein in the at least one wiring region the second layer of metal serves as a via interconnecting two metal wires as recited in claim 7, there is inadequate description in the disclosure for at least one wiring region that lies to the periphery of the metal stacked inductor.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al., US patent No. 6,395,637.

Regarding claim 1, Park teaches (fig. 4E) a semiconductor structure comprising a high performance metal stacked inductor having a relatively low sheet resistance (col. 6, lines 18-21), the metal stacked inductor comprising at least one first layer of metal (12) which serves as an upper metal wire in the semiconductor structure and a second layer of metal (15) located directly on top of the first layer of metal.

Regarding claim 2, Park teaches (fig. 4E) the entire claimed structure of claim 1 above including a third metal layer (21a) located directly on top of the second layer of metal (15).

Regarding claims 3 and 4, Park teaches (fig. 4E) the entire claimed structure of claims 1 and 2 above including the metal-stacked inductor is spiral shaped (col. 5, lines 37-40).

Regarding claim 5, Park teaches (col. 5, lines 41-47) the entire claimed structure of claim 1 above including the first layer of metal is connected to a lower metal wiring level.

Regarding claim 6, Park teaches (col. 5, lines 41-47) the entire claimed structure of claim 1 above including the lower metal wiring level comprises a wiring region embedded within an interconnect dielectric (11).

Regarding claim 7, Park teaches (fig. 4E) the entire claimed structure of claim 1 above including at least one wiring region (15) that lies to the periphery of the metal stacked inductor, the wherein in the at least one wiring region the second layer (15) of metal serves as a via interconnecting two metal wires (12) and (21a).

Regarding claim 19, Park teaches (fig. 4A 4E) a method of forming a semiconductor structure comprising: providing a partial interconnect structure comprising a lower metal wiring level located on a substrate (col. 5, lines 41-47); forming a first dielectric material (11) on the partial interconnect structure; forming a first layer of metal (12) in the first dielectric material, the first layer of metal serves as an upper metal wire of the interconnect structure and as the bottom layer of a metal stacked inductor; and forming a second layer of metal (15) on the first metal layer.

Park teaches (col. 5, lines 41-47) forming active device structure such as CMOS before forming the inductor structure. Furthermore Park teaches forming contact holes (not shown) to form contact area by patterning the dielectric layer (11) and the first metal later (12). Therefore the first metal layer (12) is capable of serving as an upper metal wire of the interconnect structure and as the bottom layer of the metal stacked inductor.

Regarding claim 20, Park teaches the entire claimed structure of claim 19 above including forming a third layer of metal (21a) directly on top of the second layer of metal (15).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al.

Regarding claim 8, Park teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the first layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3.0 micro-ohm*cm or less.

6. Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Chaudhry et al. US patent No. 6,639,298.

Regarding claims 9 and 10, Park teaches substantially the entire claimed structure of claims 1 and 8 above except explicitly stating that the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

It is conventional and also taught by Chaudhry (fig. 9) using Cu in the process of forming a multi-layer inductor structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper in the structure of Park as taught by Chaudhry in order to form a high Q inductor.

Regarding claims 11-13, Park teaches substantially the entire claimed structure of claims 1 and 10 above including the second layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro-ohm*cm or less and the second layer of metal is Al and is different conductive material as the first metal layer. Since the claimed material is the same as Park, Park's material inherently has resistivity of about 3 micro-ohm*cm or less. Furthermore since Chaudhry teaches the first metal layer to be copper, the combined structure of Park and Chaudhry teaches the first conductive material different than the second metal layer.

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Regarding claims 14-16, Park teaches (col. 6, lines 1-8) substantially the entire claimed structure of claims 1 and 2 above including the third layer of metal is aluminum having a resistivity of about 3 micro-ohm*cm or less, the third layer of metal is different conductive material as the first or second layers of metal.

Regarding claim 17, Park teaches substantially the entire claimed structure of claims 1 and 10 above including the first layer of metal is comprised of Cu and the second metal layer is comprised of Al (fig. 2C of Park).

Regarding claim 18, the combined structure of Park and Chaudhry teaches substantially the entire claimed structure of claims 2, 10 and 14 above including the first layer of metal is comprised of Cu, the second layer of metal is comprised of Cu and the third layer of metal is comprised of Al.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

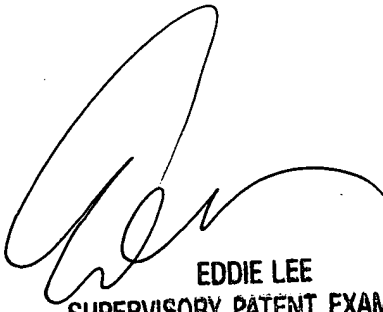
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG

November 11, 2004



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800